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09/827,676	04/06/2001	Tsutomu Tanaka	09792909-4970	6747

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,676	TANAKA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-9,11,13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-9,11,13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 3 are objected to because of the following informalities: Claims 1 and 3 were nonelected claims, which were filed on 02/15/02. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-7 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,246,070 to Yamazaki et al. in view of US Patent No. 6,265,730 to Nakanishi et al.

Regarding claim 4, Yamazaki et al. (figures 1A-E, 2A-2E, 3, 11) teach a method of making a bottom-gate thin-film transistor comprising:

forming a gate electrode (102) on a transparent substrate (100);

forming a gate insulating film (103) on the gate electrode (102);

forming a laminate on the gate insulating film (103), comprising:

forming a precursor film (106) for an active layer, and

forming a protective insulating film (105) directly on and in physical contact with the precursor film (106) without using an etching process, the protective insulating film (105) having a thickness of about 100 nm or less (column 8, lines 31-34);

implanting a dopant when forming a source-drain region (figure 2A) of the precursor film (106) for the active layer through the protective insulating film (105) without etching the protective insulating film (105);

activating the implanted dopant so that a non-doped portion constitutes the active layer (column 11, lines 28-32); and

forming an interlayer insulating film (117) on the protective insulating film.

Yamazaki et al. differ from the claimed invention by not showing the gate insulating film comprising a silicon oxide film formed on a silicon nitride film. However, Nakanishi et al. (figure 2) teach the gate insulating film comprising a silicon oxide film (24) formed on a silicon nitride film (23). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakanishi et al. into the method taught by Yamazaki et al. because it protects the device from the external environment. The combined device shows the gate insulating film comprising a silicon oxide film formed on a silicon nitride film.

Regarding claim 5, Yamazaki et al. teach the active layer comprises a crystallized silicon film (column 9, lines 27-31). In thin film transistor (TFT), the crystallized silicon film is normally a polysilicon.

Regarding claims 6 and 7, Yamazaki et al. teach a method of making a TFT, wherein, in the laminate forming step, an amorphous silicon film is formed on the gate insulating film (103), the amorphous silicon film is crystallized to form a crystallize silicon film, and the protective insulating film (105) is formed on the crystallize silicon film (106) (column 8, lines 4-10; column 9, lines 27-31).

Regarding claim 9, Yamazaki et al. disclose a heat treatment step is conducted to activate the impurity elements in the silicon film (column 11, lines 28-32). It is inherent that the heat treatment step would also recover the defects formed in the protective insulating film. Therefore, Yamazaki et al. inherently disclose the defects formed in the protective insulating film can be recovered after the heat treatment.

Yamazaki et al. and Nakanishi et al. differ from the claimed invention by not showing the heat treatment of the protective insulating film by applying a temperature of about 600^0 C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the heat treatment of the protective insulating film by applying a temperature of about 600^0 C because it detects the defects in the protective insulating film. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Nakanishi et al., and further in view of US Patent No. 6,063,654 to Ohtani.

Regarding claim 8, the disclosures of Yamazaki et al. and Nakanishi et al. are discussed as applied to claims 4-7 and 9 above.

Yamazaki et al. differ from the claimed invention by not showing to form the oxide layer on the amorphous silicon film through thermal oxidation. However, Ohtani (figures 3A-E) teaches to form the oxide layer on the amorphous silicon film (203) through thermal oxidation (column 9, lines 23-29). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ohtani into the device

taught by Yamazaki et al. because the oxide film through thermal oxidation improves wetting of the surface of the amorphous silicon film to suppress the solution from being repelled. The combined device shows that the protective insulating film is formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is crystallized to form a crystallize silicon film.

Yamazaki et al., Nakanishi et al. and Ohtani differ from the claimed invention by not showing the surface oxidation of the amorphous silicon with temperature about 400^0 C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the surface oxidation of the amorphous silicon with temperature about 400^0 C because it improves wetting of the surface of the amorphous silicon film to suppress the solution from being repelled. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Nakanishi et al., and further in view of US Patent No. 6,281,552 to Kawasaki et al.

Regarding claim 11, the disclosures of Yamazaki et al. and Nakanishi et al. are discussed as applied to claims 4-7 and 9 above.

Yamazaki et al. and Nakanishi et al. differ from the claimed invention by not showing a transparent electrode, and an alignment layer on a protective insulating film of the bottom gate thin film transistor to comprise a TFT substrate; and interposing a liquid crystal between the TFT substrate and a counter substrate provide with counter electrode. However, Kawasaki et al.

(figure 6) teach forming an interlayer insulating film (151), a transparent electrode (161), and an alignment layer (601) on a protective spacer film of the bottom gate thin film transistor to comprise a TFT substrate; and interposing a liquid crystal (605) between the TFT substrate and a counter substrate (602) provide with counter electrode (603). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kawasaki et al. into the device taught by Yamazaki et al. and Nakanishi et al. because it displays an active matrix liquid crystal display device for light imaging. The combined device shows a transparent electrode, and an alignment layer on a protective insulating film of the bottom gate thin film transistor to comprise a TFT substrate; and interposing a liquid crystal between the TFT substrate and a counter substrate provide with counter electrode.

5. Claims 13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Nakanishi et al., and further in view of US Patent No. 6,420,758 to Nakajima and US Patent No. 6,582,837 to Toguchi et al.

Regarding claim 13, the disclosures of Yamazaki et al. and Nakanishi et al. are discussed as applied to claims 4-7 and 9 above.

Yamazaki et al. and Nakanishi et al. differ from the claimed invention by not forming an organic EL element driven by the bottom gate thin film transistor on the interlayer insulating film. However, Nakajima teaches forming an organic EL element (3045) driven by the bottom gate thin film transistor on the interlayer insulating film (3042) (see figure 21; column 23, line 24 – column 25, line 62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakajima into the method

taught by Yamazaki et al. and Nakanishi et al. because the organic EL element improves the quality of the image.

Yamazaki et al., Nakanishi et al. and Nakajima further differ from the claimed invention by not showing the EL element including a luminescent layer sandwiched between a first pair of layers comprising an anode layer and a hole-transporting layer and a second pair of layers comprising an electron-transporting layer and a cathode layer. However, Toguchi et al. (figure 1) teach the EL element including a luminescent layer (4) sandwiched between a first pair of layers comprising an anode layer (2) and a hole-transporting layer (3) and a second pair of layers comprising an electron-transporting layer (5) and a cathode layer (6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Toguchi et al. into the method taught by Yamazaki et al., Nakanishi et al. and Nakajima because it improves the quality of the image. The combined device shows the EL element including a luminescent layer sandwiched between a first pair of layers comprising an anode layer and a hole-transporting layer and a second pair of layers comprising an electron-transporting layer and a cathode layer.

Regarding claim 15, the combined device shows the forming of the organic EL comprises forming the cathode layer, forming the electron-transporting layer, forming the luminescent layer, forming the hole-transporting layer, and forming the anode layer, in this order.

Regarding claim 16, the combined device shows the forming of the organic EL comprises forming the anode layer, forming the hole-transporting layer, forming the luminescent layer, forming the electron-transporting layer, and forming the cathode layer, in this order.

Regarding claim 17, the combined device shows the cathode layer is composed of a magnesium-indium alloy (Toguchi et al.; column 27, lines 8-12).

Regarding claim 18, the combined device shows the electron-transporting layer is a known material (Toguchi et al.; column 1, lines 47-48). The combined device differs from the claimed invention by not showing the electron-transporting layer is composed of a 10-benzoquinolinol-beryllium complex. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the electron-transporting layer is composed of a 10-benzoquinolinol-beryllium complex, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Regarding claim 19, the combined device shows the luminescent layer material is a conventional material (Toguchi et al.; column 1, lines 39-45). The combined device differs from the claimed invention by not showing the luminescent layer is composed of an 8-quinolinol-aluminum complex containing a quinacridone derivative. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the luminescent layer is composed of an 8-quinolinol-aluminum complex containing a quinacridone derivative, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Regarding claim 20, the combined device shows the hole-transporting layer is composed of TPD (4,4',4''-tris-(methylphenylphenylamino)triphenylamine) (Toguchi et al.; column 1, lines 49-51).

Regarding claim 21, the combined device shows the anode layer is composed of platinum (Toguchi et al.; column 27, lines 3-6).

Response to Arguments

Applicant's arguments with respect to claims 4-9, 11, 13 and 15-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
March 29, 2004

Steve Loke